IN THE CLAIMS:

Please AMEND claims 1, 5 and 6 in accordance with the following:

1. (Currently Amended) A digital phase locked circuit synchronizing a phase of an output clock signal with a phase of an input clock signal wherein said output clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part comparing the phase of said output clock signal with the phase of said input clock signal;

a phase comparison result detecting part outputting an increasing/decreasing (INC/DEC) request signal controlling a division operation based on a phase comparison signal from said phase comparing part;

an execution rate computing part computing a phase difference between said input clock signal and said output clock signal based on said INC/DEC request signal from said phase comparison result detecting part and outputting an execution rate corresponding to said phase difference, wherein as the phase difference increases, the execution rate is made lower, and as the phase difference decreases, the execution rate is made higher; and

a clock generating part controlling a division operation of said master clock signal in accordance with said INC/DEC request signal from said phase comparison result detecting part and changing a phase absorption speed of said output clock signal by masking said INC/DEC request signal in accordance with said execution rate from said execution rate computing part.

2. (Previously Presented) The digital phase locked circuit as claimed in claim 1, wherein said phase comparison result detecting part, comprising:

an up-down counter counting up/down when a phase comparison signal, comprising an exclusive OR signal of said input clock signal and said output clock signal from said phase comparing part, is HIGH/LOW, respectively; and

a detecting part outputting a decreasing (DEC) request signal when a minimum counter value of said up/down counter is detected and an increasing (INC) request signal when a maximum counter value of said up/down counter is detected.

3. (Previously Presented) The digital phase locked circuit as claimed in claim 1, wherein said execution rate computing part has a phase difference computing counter counting up/down a phase difference counter value thereof based on said INC/DEC request signal,

respectively from said phase comparison result detecting part and setting said phase difference counter value as a computed phase difference and a phase absorption execution rate determining part outputting an execution rate corresponding to said computed phase difference with reference to a correspondence table in which correspondence between phase differences and execution rates is stored.

4. (Original) The digital phase locked circuit as claimed in claim 3, wherein said execution rate computing part sets said computed phase difference by summing up a plurality of counter values for each predetermined time interval, the counter values computed by sampling said phase difference counter in a shorter time interval.

5. (Currently Amended) A digital phase locked circuit for synchronizing a phase of a divided clock signal with a phase of an input clock signal wherein said divided clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part comparing the phase of said output clock signal with the phase of said input clock signal;

a phase comparison result detecting part referring to a comparison result from said phase comparing part and outputting a signal increasing/decreasing a division number for dividing said master clock signal when the phase of said output clock signal proceeds forward/behind the phase of said input clock signal;

a mask processing part identifying a single applied mask rate among a plurality of mask rates for masking a part of an increasing/decreasing (INC/DEC) request signal depending on a phase difference between the input clock signal and the master clock signal, wherein as the phase difference increases, the mask rate is made lower, and as the phase difference decreases, the mask rate is made higher, masking the output signal from the phase comparison result detecting part depending on the identified mask rate, and outputting the masked signal; and

a dividing part obtaining the divided clock signal by controlling increasing or decreasing operation on the division number based on the outputted masked signal.

6. (Currently Amended) A digital phase locked circuit for synchronizing a phase of an output clock signal with a phase of an input clock signal wherein said output clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part comparing the phase of said output clock signal with the phase

of said input clock signal;

a phase comparison result detecting part outputting an increasing/decreasing (INC/DEC) request signal controlling a division operation based on a phase comparison signal from said phase comparing part;

an execution rate computing part computing a phase difference between said input clock signal and said output clock signal based on said INC/DEC request signal from said phase comparison result detecting part and outputting an execution rate corresponding to said phase difference, wherein as the phase difference increases, the execution rate is made lower, and as the phase difference decreases, the execution rate is made higher; and

a clock generating part generating the output signal to control a division operation on said master clock signal in accordance with said INC/DEC request signal from said phase comparison result detecting part, the clock generating part including a INC/DEC request mask control means and a clock generating logic, the INC/DEC request mask control means masking the INC/DEC request signal based on the execution rate supplied from the execution rate computing part so as to obtain a desired absorption characteristic, the clock generating logic generating the output signal based on the masked INC/DEC request signal.